REMARKS

Applicant's counsel thanks the Examiner for the careful consideration given the application. Claims 1 to 30 are presently pending in the application. Claims 1, 2, 8 and 14 to 24 have been further amended to more clearly and precisely define the present invention. Further, claim 24 has been amended to respond to the objection noted by the Examiner in item 2.

The present invention is directed to a CMOS active pixel sensor (APS) transducer array having a number of APS's arranged in columns and rows for sensing an image, wherein the array is adapted to decimate the image by accessing output signals only from selected APS's. The present invention is directed to an apparatus and a method wherein only the selected APS's are energized whereby power is applied to them during the entire image sensing cycle, i.e. during the cycle that includes the resetting, integration and reading of the APS. The power consumption of the APS array is reduced by energizing the selected APS's that are being used to sense an image, and de-energizing all of the other APS's. This is done by electrically connecting or disconnecting APS's from between a power supply terminal and a ground terminal for a complete image sensing cycle.

In the present disclosure and claims, an APS is considered to include all of the elements that are required to permit it to function properly. For example figure 1, illustrates a basic CMOS active pixel sensor (APS), which includes a light sensitive element 11 and three transistors 12, 14 and 16. It is noted that Wu et al illustrates the identical APS in their figure 1. Wu et al then goes on to describe their invention, which is an improved correlated double sampling APS illustrated in their figure 3. The improved APS further includes a shutter transistor M1, a PMOS transistor M2 to reduce power consumption by the APS and additional transistors in order to achieve double sampling. However, it is to be noted that in order for Wu et al's APS (figure 3) to function properly, each of the transistors M1 to M5 are switched both on and off during each image sensing cycle, and therefore each of the transistors is an integral part of Wu et al's APS.

More specifically, Wu et al disclose a basic CMOS active pixel sensor (APS) (see figure 3 and col. 2, lines 17 to 57), of the type that can be operated in a "correlated double sampling" manner and which can be used in a conventional image sensor array having rows and columns (see figure 2 and col. 2, lines 9 to 16). Wu et al further disclose a method of reducing the overall power consumption of each APS by using a PMOS transistor M2 as the reset transistor, which is operable at lower voltages due to the body effect (ie: PMOS transistors operate at lower voltages) (col. 3, lines 13 to 23). Wu et al's method allows for the operation of the imaging array at voltages of less than 2 volts. It is to be noted that Wu et al achieve power conservation on an individual APS basis.

The Examiner states in the last paragraph of item 3, that "the Examiner believes that the broadest interpretation of the present claimed invention does in fact read on the cited reference...." . Applicant has attempted to more precisely define the present invention in order to render moot the Examiner's interpretation of the former claims.

Present apparatus claims 1, 14, 17, 20 and 22 include the limitation of a switching circuit adapted to selectively connect the selected APS's between the power terminal and the ground terminal for a complete image sensing cycle (emphasis added), i.e. power is applied to the selected uring the entire sensing cycle. On the other hand, Wu et al's figure 3 illustrates transistors M2 and M4 that are used to carry out the functions of the APS rather then to energize or de-enegize the APS for an entire cycle. Transistors M2 and M4 are integral to the APS component. It is therefore respectfully submitted that Wu et al does not teach or infer an array in which only selected APS's are energized, but that all APS's are connected to the power supply. Further, claims 2, 8, and 14 to 23 define various arrangements of switches adapted to energize only the selected APS's.

Though Lee et al teach an image decimation technique, they do not teach or infer an APS array in which only the selected APS's that are being accessed are being energized by connecting them to a power supply. It is noted that the Examiner indicates his agreement with this in the third paragraph of his item 3.

In item 5, The Examiner rejected claims 1-23 under 35 USC 103(a) over Wu et al (US 6,111,245) in view of Lee et al (US 6,466,265). For the reasons stated above, this rejection is respectfully traversed. In summary, it is submitted that Wu et al teach an APS having transistors, such as M2 and M4, which are an integral to the APS to carry out its function, and do not teach an APS having the means for energizing or de-energizing it for its entire image sensing cycle. Further, though Lee et al teach an image decimation technique, they do not teach or infer energizing or de-energizing selected APS's. Therefore combining Wu et al with Lee et al would only provide the obvious result of an APS array that can operate using an image decimation technique in which the array would consist of correlated double sampling APS's, as illustrated in figure 3, that can operate in a low voltage environment .

The Examiner is therefore respectfully requested to withdraw his rejection of claims 1 to 23 under 35 USC 103(a).

Claim 24 specifically defines a unique method of operating an array. The method comprises determining the selected APS's to be accessed to sense an image, energizing the selected APS's and de-energizing the APS's that are not selected.

Though the Examiner does not specifically reject claims 24 to 30 in his item 5, the Examiner refers to claims 24 to 30 on pages 14 to 16 of the Action. Present claims 24 to 30 are directed to a unique method of controlling an array of APS's that uses an image decimation technique. In his discussion of claim 24 on page 14, the Examiner states at the bottom of page 14 that "Furthermore, Wu fails to teach the step of:

a. determining the selected APS's having outputs that are decimated; and

b. disconnecting the selected APS's from the power supply.",

which is the method being claimed. The Examiner further states that Lee et al teach an image decimation technique and therefore the combination would provide a "sensor with random addressability, thus providing a more versatile multiple array for achieving high pixel rate data transfers." Though Wu et al's APS's might be used in arrays using Lee et al's image decimation technique, it is respectfully submitted that the teachings of Wu et al in view of Lee et al do not render claims 24 to 30 obvious to a person having ordinary skill in the art and the Examiner is respectfully requested to withdraw his rejection of claims 24 to 30.

In view of the above amendments and remarks, and having dealt with all of the matters raised by the Examiner, early and favourable reconsideration of the application on its merits is respectfully requested.

If any further fees are required by this communication, please charge such fees to our Deposit Account No. 16-0820, Order No. 33728.

Respectfully submitted,
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